REMARKS/ARGUMENTS

Favorable reconsideration of this application as presently amended and in light of the following discussion is respectfully requested.

Claims 1, 4-7, 10-13 and 16-28 are presently active in this case, Claims 1, 7, 10, 13, 20 and 24 having been amended, Claim 15 canceled and Claims 26-28 added by the present Amendment, Claims 2, 3, 8, 9 and 14 having been previously canceled.

In the outstanding Official Action Claims 1, 4-6, 13 and 22 were rejected under 35 USC §103(a) as being unpatentable over Nowak et al (US Patent 6,191,451). Claims 7, 10-12 and 15 were rejected under 35 USC §103(a) as being unpatentable over Nowak as applied to Claim 1 above, and further in view of Stolmeijer et al. and Claims 16-19 were allowed.

Applicants' acknowledge with appreciation the allowance of Claims 16-19.

New Clams 26-28 are submitted herewith and find clear support in Applicant's Figure 1 disclosure, for example. No new matter has been added.

In light of the citation of new prior art in regard to Claim 1, Claim 1 has been amended to further clarify the claimed invention. To that end, amended Claim 1 recites first and second areas in a well area are separated by an element isolation area, and the first and second conductivity type semiconductor layers formed in the first and second areas configure a capacitor. A low resistance area formed at the base portion of the well area connects the first and second areas. The low resistance area has a resistive value lower than that of the well area. Since the first and second areas configuring a capacitor are connected to each other by the low resistance area, the well resistance can be kept low even when the distance between the first and second conductivity type semiconductor layers is broadened. In addition, the low resistance area is not in contact with the depletion layers of the junction portions between each semiconductor layer and the well area, but is in contact with the

element isolation areas. Therefore, the resistive value of a portion under the isolation areas can be lowered. As a result, the well resistance can be kept low even when the width of the element isolation areas is broadened. Thus, thermal noise can be prevented and power loss introduced by the well resistance can be suppressed.

Claim 7 has also been amended to clarify that first and second areas in a first well area are separated from each other by an element isolation area, a MOS transistor is formed in the first area, and a first semiconductor layer is formed in the second area. A first low resistance area formed at a base portion of the first well area connects the first and second well areas. The first low resistance area has a resistive value lower than that of the first well area. Therefore, since the first semiconductor layer formed in the second area and the MOS transistor formed in the first area are connected to each other by the first low resistance area, the parasitic resistance of the first well area can be reduced. As a result, the potential supplied to the first semiconductor layer can be supplied to the well area without a loss, a high-gain amplifier can be constructed.

Claim 13 has been amended to recite first and second areas in the first well area are separated from each other by the element isolation area, and a first electrode of a bipolar transistor is formed on the first area. A second electrode is formed on the first electrode. A third electrode of the bipolar transistor is formed on the second electrode. A first low resistance area formed at a base portion of the first well area connects the first and second areas. The first low resistance area has a resistive value lower than that of the well area. Therefore, since the third electrode formed in the second area and the first and second electrodes formed on the first area are connected to each other by the first low resistance area, the parasitic resistance of the first well area can be reduced. Accordingly, the power loss of the bipolar transistor can be suppressed, and a high-gain amplifier can be constructed.

Turning now to the newly cited prior art, Nowak et al. disclose an improved decoupling capacitance of SOI device. In FIG. 2 of Nowak et al., N-wells 132, 134 are formed in the bulk area 130, and isolation layers 20 are formed in the N-wells 132, 134 and the bulk area 130. N+ regions 136, 144 and P+ regions 138, 142, which are separated by the isolation layers 20 are formed in the N-wells 132, 134 and bulk area 130. The outstanding Office Action states the finding that the P+ implant 140 of Nowak et al. corresponds to the low resistance area of Applicant's invention. However, as recognized in the first sentence at page 3 of the outstanding Office Action, the P+ implant 140 is not in contact with the isolation layers 20. Moreover, pending Claims 1, 7 and 13 recite that the low resistance area connects the first and second areas which are separated by an element isolation area, while Nowak et al. do not suggest such structure. That is, in the Nowak et al. patent, the areas in which the N+ regions 136 and P+ regions 138 are formed are connected to each other by the N-wells 132, but are not connected by the low resistance area. Thus, Nowak et al. do not suggest the structure of the claimed invention by which the resistive value of the portion under the element isolation areas is lowered, and do not suggest the advantages of preventing the occurrence of thermal noise and reducing the power loss as achieved according to the claimed invention.

In addition, Nowak et al. do not suggest a MOS transistor, bipolar transistor or analog circuit formed in the N+ regions or P+ region 138.

Accordingly, for the reasons above noted, it is respectfully submitted that Nowak et al. do not suggest or render obvious the subject matter stated in pending amended Claims 1, 7 or 13. Accordingly, the outstanding rejection on the merits is traversed..

Consequently, in view of the present amendment, independent Claims 1, 7 and 13 and the remaining claims dependent therefrom, in addition to Claim 16-19, are believed to be

patentably distinguishing over the applied prior art and in condition for allowance. An early and favorable action to that effect is respectfully requested.

Respectfully submitted,

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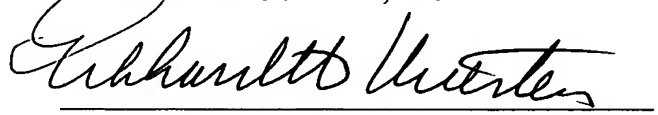

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